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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/299,659	04/27/1999	YUTAKA TERADA	43889-861	3538

20277 7590 03/28/2003  
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WASHINGTON, DC 20005-3096

EXAMINER

FAN, CHIEH M

ART UNIT	PAPER NUMBER
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2634

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/299,659

Applicant(s)

TERADA ET AL.

Examiner

Chieh M Fan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 January 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-5, 8 and 9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4 and 8 is/are allowed.
- 6) ☒ Claim(s) 3, 5 and 9 is/are rejected.
- 7) ☒ Claim(s) 2 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 03 January 2003 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Drawings***

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 1/3/03 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the first delay circuit defines the delay time based on the result of comparison performed by the comparator" in lines 1-2. It is not clear whether "the result of comparison" is referred to the result of comparison between one of the leading edges of the data signal and the edge of the clock signal (see lines 10-11 of claim 4) or to the result of comparison between one of the trailing edges of the data signal and the edge of the clock signal (see lines 13-14 of claim 4). Similarly, it is not

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clear the limitation "the result of comparison performed by the comparator" recited in line 4 of claim 9 is referred to which result of comparison. According to Fig. 1 of the instant application, the examiner suggests that the limitation "the first delay circuit defines the delay time based on the result of comparison performed by the comparator" recited in lines 1-2 of claim 9 should be changed to --- the first delay circuit defines the delay time based on the result of comparison, performed by the comparator, between one of the leading edges of the data signal and the edge of the clock signal ---.

Similarly, the limitation "the second delay circuit defines the delay time based on the result of comparison performed by the comparator" recited in lines 3-4 of claim 9 should be changed to --- the second delay circuit defines the delay time based on the result of comparison, performed by the comparator, between one of the trailing edges of the data signal and the edge of the clock signal ---.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical

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Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 3 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki (U.S. Patent No. 5,952,857).

Regarding claim 3, Suzuki teaches an input circuit (Fig. 1, col. 2, lines 66-67, also see col. 3, line 24 through col. 5, line 8) comprising:

delay means (13-1 and 14 in Fig. 1, col. 3, line 24 through col. 4, line 28) for defining a delay time for at least one logical state of a data signal (signal A or B in Fig. 1) and thereby delaying a clock signal for the delay time defined; and

a holding circuit (15-1 or 15-2 in Fig. 1) for holding the data signal responsive to the delayed clock signal (CLK1 in Fig. 1);

wherein the delay means comprises:

a comparator (20 in Fig. 1) for comparing the edge of the clock signal, on which the data signal is intended to be latched, to at least one of leading and trailing edges of the data signal (output of 12 in Fig. 1, note that the output of the NAND gate 12 indicates the signal with largest delay among the n input signals, i.e., among the signals A and B; see col. 3, lines 52-62. Therefore, the edge of the output of the NAND gate represents the edge of the signal A or B, depending on which signal has a larger delay); and

a delay circuit (22 and 14 in Fig. 1) for defining the delay time based on a result of comparison performed by the comparator (see 21 in Fig. 1).

Regarding claim 5, Suzuki further teaches that the delay circuit (22 and 14 in Fig. 1) defines the delay time based on the result of comparison performed by the comparator (20 and 21 in Fig. 1) and a setup time ("Ts" at the bottom of Fig. 2F, also see col. 4, lines 25-31) for correctly latching the data signal.

***Allowable Subject Matter***

6. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 2 is allowable over the prior art of record because the prior art of record does not teach or suggest that the delay time is defined such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

7. Claims 4 and 8 are allowed. Claim 9 would be allowable if rewritten to overcome the rejection under 35 USC 112, second paragraph above.

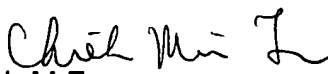
Claims 4, 8 and 9 are allowable over the prior art of record because the prior art of record does not teach or suggest the limitations recited in "a first delay circuit", "a second delay circuit" and "a selector" of claim 4.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M Fan whose telephone number is (703) 305-0198. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703) 305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

  
Chieh M Fan  
Examiner  
Art Unit 2634

cmf  
March 22, 2003